Cummins College of Engineering for Women

(An autonomous institute affiliated to Savitribai Phule pune university)

Karve Nagar, Pune - 411 052.

Vision

To be globally renowned engineering institute for imparting holistic education and developing professional women leaders in engineering and technology

Syllabus Structure and Syllabus

of

B.Tech. (Honors) in VLSI Technology (Electronics and Telecommunication Engineering)

2023 Pattern [R0]

List of Abbreviations

Abbreviation	Title
PCC	Programme Core Course
BSC	Basic Science Course
ESC	Engineering Science Course
PE	Programme Elective Course
OE	Open Elective
VSEC	Vocational and Skill Enhancement Course
CC	Co-curricular Courses / Liberal Learning Course
IKS	Indian Knowledge System
VEC	Value Education Course
RM	Research Methodology
INTR	Internship
PROJ	Project
CEP	Community Engagement Project
RM	Research Methodology
Mm	Multidisciplinary Minor
AEC	Ability Enhancement course

Curriculum for Honors Degree Programme
in
VLSI TECHNOLOGY
in B. Tech. Electronics and Telecommunication Engineering
(Academic Year: 2025-26 Onwards)

Course Code	Course Title	Teaching Scheme Hours / Week			Cr	Examination Scheme			Total Marks
		L	T	P		ISE	ESE	Pr/Or	
23HVL501	Digital CMOS Circuit Design	3	0	0	3	50	50	0	**100**
23HVL502	Physical IC Design	3	0	0	3	50	50	0	**100**
23HVL501L	Digital CMOS Circuit Design Lab	0	0	2	1	25	0	25	**50**
23HVL601	System Verilog for Verification	3	0	0	3	50	50	0	**100**
23HVL602	CMOS Analog and Mixed Circuit Design	3	0	0	3	50	50	0	**100**
23HVL601L	System Verilog for Verification Lab	0	0	2	1	25	0	25	**50**
23HVL602L	CMOS Analog Circuit Design Lab	0	0	2	1	25	0	25	**50**
23HVL801	Design for Testability	3	0	0	3	50	50	0	**100**
	Total =	**15**	**0**	**6**	**18**	**325**	**250**	**75**	**650**

L=Lecture, T=Tutorial, P= Practical, Cr= Credits, ISE =In Semester Evaluation, ESE =End Semester Examination, Pr/Or = Practical/Oral

APPROVED BY
Secretary Academic Council
MKSSS's Cummins College of Engineering
For Women, Pune-411052

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23HVL501 DIGITAL CMOS CIRCUIT DESIGN

Teaching Scheme
Lectures: 3 Hours / Week

Examination Scheme
ISE: 50 Marks
ESE: 50 Marks
Credits: 3

Prerequisite: Digital Electronics

Course Objectives:
1. To provide knowledge of circuit models for analysis of digital CMOS circuits and interconnect.
2. To explain implementation technique necessary to realize CMOS circuits/ Sub-systems using various CMOS logic structures.
3. To explain Computation methods required for circuit characterization and performance estimation.
4. To make them understand various CMOS processes and emerging nanometers-scale technologies

Course Outcomes:
After completion of the course, students will be able to
CO1 Analyze MOS and CMOS based logic circuit.
CO2 Analyze the performance parameter of CMOS logic circuit.
CO3 Design moderately sized CMOS circuits/ sub-systems for various CMOS Logic structures.
CO4 Describe the fundamentals of BiCMOS logic circuits

Unit I: Fundamentals of CMOS Logic
Types and principles of MOSFETs. MOS Inverters, Static and Dynamic characteristics, Resistive, Depletion and Enhancement load NMOS inverters, the basic CMOS inverter, voltage transfer characteristics, logic threshold, Noise margins. Second order effects in MOSFETs. Dynamic behaviour, transition time, Propagation Delay, Power Consumption.

Unit II: CMOS Layout Fundamentals
Technology scaling, MOS Circuit Layout, Stick diagrams, Layout design rules, MOS device layout, Inverter layout, CMOS-circuits layout, Circuit Compaction, Euler's Rule.

Unit III: Static and Dynamic Logic
Combinational MOS Logic Design, Static MOS design, Complementary MOS, Ratioed logic, Pass Transistor logic, Transmission gate logic and circuits. Dynamic MOS design, Dynamic logic families and their performance.

Unit IV: CMOS Memory
MOS Memory design, Design of ROM, SRAM and DRAM cells, Sequential MOS Logic Design, Static and dynamic latches, flip flops & registers.

Unit V: Bi-CMOS Logic
Introduction to low power design, Input and Output Interface circuits. BiCMOS Logic Circuits, Introduction, Basic BiCMOS Circuit behavior, Switching Delay in Bi-CMOS Logic circuits.

Text Books:
1. S.M. Kang & Y. Leblibici, **"CMOS Digital Integrated Circuits-Analysis & Design"**, *McGraw-*

Hill, (3rd edition), (2003).
2. Jan M. Rabaey, Anantha P.Chandrakasan, BorivojeNikolić, **"Digital Integrated Circuits: A Design Perspective"**, *Pearson Education*, (2nd Edition), (2003).

Reference Books:

1. Neil Weste& K. Eshraghian,**"Principles of CMOS VLSI Design: A Systems Perspective"**, *McGraw Hill Pub*., (1985).
2. Douglas Pucknell, Kamran Eshraghian, **"Basic VLSI Design"**, *PHI*., (3rd Edition), (2013).

Online Resources:

1. https://onlinecourses.nptel.ac.in/noc20_ee29/preview
2. https://onlinecourses.nptel.ac.in/noc20_ee05/preview

23HVL502 Physical IC Design

Teaching Scheme
Lectures: 3 Hours / Week

Examination Scheme
In Semester: 50 Marks
End Semester: 50 Marks
Credits: 3

Course Objectives:

1 To understand the VLSI physical design flow, impact of various design styles in physical implementation.
2 To learn physical design concepts, including partitioning, floor planning, placement, routing, and timing analysis
3 To identify objectives of steps of physical design and optimization of parameters to achieve it
4 To develop problem-solving skills to tackle complex challenges in physical design, such as timing closure and signal integrity.

Course Outcomes:

After completion of the course, students will be able to

CO1 Explain physical design flow and design style-based variations in it.
CO2 Model structural representation of VLSI digital system into graph structure at various stages of the physical design flow
CO3 Apply partitioning and floor planning algorithms to optimize layout of circuit components on the chip
CO4 Analyse VLSI placement and routing problems to minimize objective functions

Unit I: Introduction to Physical Design

Introduction to VLSI Design flow, VLSI Physical Design, VLSI Design Styles, Complexity Analysis for Algorithms, Graphs for Physical Design, Graph Terminology, Graph searching Algorithms, Spanning Tree and Shortest Path Algorithms.

Unit II: Partitioning, Chip Planning and Pin Assignment

Introduction to Partitioning, Partitioning Algorithms, Kernighan – Lin (KL) Algorithm, Fidducia-Mattheyeses(FM) Algorithm, Introduction to Floor planning, Floor planning Representations: Floorplan to Constraint Graph Pair, Sequence Pair to Floorplan, Floorplan to Sequence Pair Floor Planning Algorithms: Floorplan Sizing, Cluster Growth, Simulated Annealing, Pin Assignment and Power - Ground Routing,

Unit III: Placement and Clock Tree Synthesis

Level of Placement, Design Style Specific Placement, Wirelength Estimation, Maximum Cut Size, Min-cut Placement Algorithm: Using KL and FM algorithm, Terminal Propagation, Quadratic Placement, Force Directed Placement Legalization and Detailed Placement. Design Consideration and Delay Calculation for Clock Tree, Clock Skew, Clock Routing Algorithms,

Unit IV: Global and Detailed Routing

Global Routing Introduction and Optimization Goals Single net routing (Rectilinear routing), Global, Routing in the connectivity graph, Finding Shortest Paths with Dijkstra's Algorithm, Full-Netlist Routing, Introduction Detailed Routing, Channel Routing Algorithms, Switchbox and Over the cell routing,

Unit V: Timing Closure and Physical Verification

Overview of Timing Analysis, Timing Arcs and Unateness, Delay Parameters of Combinational Circuits, Delay Parameters of Sequential Circuit, Timing Analysis in Sequential Circuit, STA in Sequential Circuit with Clock Skew, STA in Sequential Circuit with Clock Jitter, STA for Combinational Circuits, Optimizations for Physical Verification: Extraction, LVS, ERC, DRC, ECO, Antenna Check and Sign-off

Text Books:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2022, 2nd Edition.
2. Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd Ed., Kluwer.

Reference Books:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley-India.
2. J. Bhasker and Rakesh Chadha, "Static Timing Analysis for Nanometer Designs A Practical Approach, Springer 2009

Online Resources:

1. NPTEL course VLSI Physical Design
   https://onlinecourses.nptel.ac.in/noc25_cs73/course
2. NPTEL course VLSI Physical Design with timing analysis
   https://onlinecourses.nptel.ac.in/noc24_ee77

23HVL501L DIGITAL CMOS CIRCUIT DESIGN LAB

Teaching Scheme
Practical: 2 Hours / Week

Examination Scheme
ISE : 25 Marks
ESE: Oral :25 Marks
Credits: 1

Course Objectives:

1. To explain implementation technique necessary to realize CMOS circuits/ Sub-systems using CMOS process.
2. To design layout for Digital circuit using given CMOS Process.
3. To use software for simulation of layout.

Course Outcomes:

After completion of the course, students will be able to

CO1 Model digital components in given CMOS process to estimate their performance.
CO2 Design the layout of digital circuits using given CMOS process.
CO3 Simulate the layout of digital circuits in given CMOS process
CO4 Analyze and compare the performance of digital circuits to estimate their performance.

List of Experiments:

1. Design the layout for CMOS combinational circuit.
2. Design the layout for CMOS circuit using transmission gates.
3. Design the layout for CMOS sequential circuit.
4. Design the layout for CMOS 1-bit SRAM Cell.
5. Mini-Project

23HVL601 SYSTEM VERILOG FOR VERIFICATION

Teaching Scheme
Lectures: 3 Hours / Week

Examination Scheme
ISE: 50 Marks
ESE: 50 Marks
Credits: 3

Prerequisite: Knowledge of Digital Electronics, Verilog hardware description language

Course Objectives:
1. To introduce verification methologies for IC
2. To explore System Verilog for design and verification of Digital Systems
3. To introduce OOPs features for writing testbenches
4. To elaborate randomization, assertions, functional coverage and code coverage in System Verilog

Course Outcomes:
After completion of the course, students will be able to

CO1 Describe fundamental of verification in chip design
CO2 Apply the System Verilog capabilities for RTL design and synthesis
CO3 Use the System Verilog features and capabilities for design verification
CO4 Apply OOP's and Advanced OOP's concept for more effective and efficient verification

Unit I: Verification Fundamentals
The Verification Process, The Verification Plan, The Verification Methodology, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench, Building a Layered Testbench, Simulation Environment Phases, Maximum Code Reuse, Testbench Performance.

Unit II: Fundamentals of System Verilog
Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Expression Width, Net Types,
Procedural Statements, Tasks, Functions, and Void Functions, Task and Function, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

Unit III: OOP and Testbenches
OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects, Public vs. Private,
Building a Testbench, Separating the Testbench and Design, Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.

Unit IV: Randomization, Threads and Inter-Process Communication
Randomization in System Verilog, Constraint Details, Controlling Multiple Constraint Blocks, In-line Constraints, pre_randomize and post_randomize Functions, Common Randomization Problems, Iterative and Array Constraints, Random Control, Random Generator.
Working with Threads, Interprocess Communication, Events, Semaphores, Mailboxes, Building a Testbench with Threads and IPC.

Unit V: Functional Coverage and Advanced OOP
Introduction to Inheritance, Factory Patterns, Type Casting and Virtual Methods, Composition, Inheritance, and Alternatives, Copying an Object, Callbacks.
Coverage Types, Functional Coverage Strategies, Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Coverage Options, Parameterized Cover Groups, Analyzing Coverage Data.

Text Books:
1. Chris Spear, **"System Verilog for Verification"**, *Springer,* (2nd Edition), (2008).
2. Donald Thomas, **"Logic Design and Verification using System Verilog",**(2nd Edition), (2008).

Reference Books:
1. Pong P.Chu, **"FPGA Prototyping by System Verilog Example",** *Wiley,*(2nd Edition), (2018).
2. Jinck Bergeron, **" Writing Testbenches using System Verilog"**, *Springer*, (1st Edition), (2016).

Online Resources:
1. https://www.chipverify.com/systemverilog/systemverilog-tutorial
2. https://verificationguide.com/systemverilog/systemverilog-tutorial/

23HVL602 CMOS ANALOG AND MIXED SIGNAL CIRCUIT DESIGN

Teaching Scheme	**Examination Scheme**
Lectures: 3 Hours / Week	ISE: 50 Marks
	ESE: 50 Marks
	Credits: 3

Prerequisite:

Course Objectives:

1. To explore MOS capabilities for Analog circuit design
2. To utilize MOS transistor for designing analog sub-circuits
3. To explore MOS based amplifier typologies
4. To explain Mixed-signal circuits used in signal processing

Course Outcomes:

After completion of the course, students will be able to

CO1 Analyze the low frequency, high frequency MOS models and calculate various parameters
CO2 Design MOS based analog sub-circuits and calculate performance parameter
CO3 Analyze MOS based amplifier structure and calculate performance parameter
CO4 Describe mixed signal sub-circuits

Unit I: Introduction to Analog VLSI

Analog integrated circuit design, Circuit design consideration for MOS, challenges in analog circuit design, Recent trends in analog VLSI circuits, Analog MOSFET Modelling: MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, Temperature effects in MOSFET, Noise in MOSFET.

Unit II: CMOS Analog Sub-Circuits

Current Source, current Sinks, MOS Diode/Active resistor, Basic current mirrors, Advance current mirror, Current and Voltage references, Bandgap references.

Unit III: CMOS Amplifiers

Performances matrices of amplifier circuits, Common source amplifier, Common gate amplifier, Cascode amplifier, Frequency response of amplifiers and stability of amplifier.

Unit IV: CMOS Differential Amplifier

Differential signaling, source coupled pair, Current source load, Common mode rejection ratio, CMOS Differential amplifier with current mirror load.

Unit V: CMOS Operational Amplifier

Block diagram of Op-amplifier, characteristics of Op-Amplifier, Analysis of two stage Op-Amplifier, Frequency response of Op-Amplifier, CMOS Op-amp applications: Op-amp as a comparator, ADC, DAC.

Text Books:

1 P.E. Allen and D.R.Holberg, **"CMOS Analog Circuit Design"**,*Oxford University Press*, (3rd Edition), (2012).
2 R.Gregorian and G.C.Temes, **"Analog MOS Integrated Circuits for Signal Processing"**,*John*

Wiley and Sons,(1986).

Reference Books:

1. B. Razavi, **"Design of Analog CMOS Integrated Circuits",***Tata McGraw-Hill* , (2nd Edition), (2002).
2. R.J.Baker, H. W. Li, D. E. Boyce,**"CMOS Circuit Design, Layout, and Simulation",** *PHI*, (2nd Edition), (2006).

Online Resources:

1. https://onlinecourses.nptel.ac.in/noc21_ee51/preview

23HVL601L SYSTEM VERILOG FOR VERIFICATION LAB

Teaching Scheme
Practical: 2 Hours / Week

Examination Scheme
ISE : 25 Marks
ESE: Oral :25 Marks
Credits: 1

Course Objectives:

1. To explore System Verilog for design and verification of Digital Systems
2. To explain OOPs features for writing testbenches
3. To elaborate randomization, assertions, functional coverage and code coverage in System Verilog
4. To demonstrate the software features available in lab for design Verification

Course Outcomes:

After completion of the course, students will be able to

CO1 Use the features and capabilities of the System Verilog for verification

CO2 Create and configure reusable, scalable, and robust test-benches using System Verilog

CO3 Use OOP's features to develop a complete verification environment

CO4 Integrate System Verilog components to create layered test bench structure

List of Experiments:

1. Verification of the combinational circuit.
2. Verification of the sequential circuit
3. Verification of the Finite state Machine based circuit.
4. Verification of the single port RAM .
5. Mini-Project

23HVL602L CMOS ANALOG AND MIXED SIGNAL CIRCUIT DESIGN LAB

Teaching Scheme	**Examination Scheme**
Practical: 2 Hours / Week	ISE : 25 Marks
	ESE: Oral :25 Marks
	Credits: 1

Course Objectives:

1. To explore MOS capabilities for Analog circuit design
2. To utilize MOS transistor for designing analog sub-circuits
3. To exploreMOS SPICE Model
4. To design and simulate analog integrated circuits using given CMOS process

Course Outcomes:

After completion of the course, students will be able to

CO1 Model analog components in CMOS process to estimate their performance in circuits
CO2 Design and simulate the analog sub-circuits using given CMOS process
CO3 Design and simulate the amplifier circuits using given CMOS process
CO4 Analyze and compare the performance of CMOS circuits

List of Experiments:

1. Design the MOS based current mirror circuit
2. Design the bandgap referenced circuit.
3. Analyze the performance of CMOS differential amplifier for various load.
4. Analyze the performance of two stage Op-Amp circuits.
5. Mini-Project

23HVL801 DESIGN FOR TESTABILITY

Teaching Scheme	**Examination Scheme**
Lectures: 3 Hours / Week	ISE: 50 Marks
	ESE: 50 Marks
	Credits: 3

Prerequisite: Knowledge of Digital Electronics

Course Objectives:
1. To explain need of testability
2. To explore test methodologies for computational and sequential circuits
3. To elaborate testing mechanism for CMOS circuits
4. To explore BIST and modern testing techniques

Course Outcomes:
After completion of the course, students will be able to
CO1 Use the concepts of testing to design a better yield in IC design.
CO2 Analyze the various test generation methods for static & dynamic CMOS circuits.
CO3 Analyze the design for testability methods for combinational & sequential circuits
CO4 Use the BIST techniques for improving testability.

Unit I: Basics of Testing
Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits, Current sensing-based testing, Classification of sequential ATPG methods, Fault collapsing and simulation.

Unit II: Universal Test Sets
Pseudo-exhaustive and iterative logic array testing, clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

Unit III: CMOS testing
Testing of static and dynamic circuits, Fault diagnosis, Fault models for diagnosis, Cause- effect diagnosis and Effect-cause diagnosis.

Unit IV: Design for testability
Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Unit V: Built-in self-test
Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books:

1. N. Jha & S.D. Gupta, ***"Testing of Digital Systems"***,*Cambridge,*(2003).
2. W. W. Wen, **"VLSI Test Principles and Architectures Design for Testability"**,*Morgan Kaufmann Publishers,*(2006).

Reference Books:

1. Michael L. Bushnell &Vishwani D. Agrawal, **"Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits"**,*Kluwar Academic Publishers*, (2000).
2. P. K. Lala, ***"Digital circuit Testing and Testability"***,*Academic Press*, (1st Edition), (1997).
3. M. Abramovici, M. A. Breuer, and A.D. Friedman, ***"Digital System Testing and TestableDesign"***,*Computer Science Press*, (1990).

Online Resources:

1. https://onlinecourses.nptel.ac.in/noc20_ee76/preview